Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.090”**

**.086”**

**GC**

**FBP**

**FBN**

**GA**

**GB**

**V REF**

**P OUT**

**P VDD**

**TEMP**

**N.C.**

**P GND**

**VDD**

**OUTR**

**OUT**

**DON**

**GD**

**INN**

**DOP**

**INP**

**0 ADJ**

**GND**

**SG0611c**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0035” X .0035”**

**Backside Potential: Substrate Must be connected to GND**

**Mask Ref: SG0611c**

**APPROVED BY: DK DIE SIZE .086” X .090” DATE: 8/25/21**

**MFG: SGA THICKNESS .019” P/N: SG0611**

**DG 10.1.2**

#### Rev B, 7/1